

SCOPE OF CLAIMS

Sub a'
fig. 1
1. A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others; and

said well in each of said semiconductor elements is provided with a substrate terminal through a contact hole formed therein at a region other than said source region and drain region.

Sub C'
2. The semiconductor device of Claim 1, wherein operating characteristics are changed by adjusting impurity concentration in said channel region and levels of a high voltage and a low voltage applied to said gate terminal and substrate terminal.

3. The semiconductor device of Claim 1, wherein said semiconductor layer in each of said semiconductor elements is electrically separated from each other by

means of an oxide film.

figs. 7-9

4. A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others;

said semiconductor layer is composed of a shallow well region, a heavily doped region for reducing resistance of said shallow well region, and a deep well region, which are sequentially layered in a vertical direction; and

said semiconductor layer is provided with a substrate terminal through a contact hole at a region other than said source region and drain region.

5. The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is electrically separated from the others by means of a separation region; and

a depth of said separation region is set at least as

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fig. 10

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drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

8. The semiconductor device of Claim 6, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

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figs. 11, 11A, 11B
P, 27

9. The semiconductor device of Claim 7, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

Subt a³
10. The semiconductor device of Claim 1, wherein:
each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

fig. 12
a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a

second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

11. The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

12. The semiconductor device of Claim 10, wherein:

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figs. 13(a), 13(b)
P, 30

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential.

13. The semiconductor device of Claim 11, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in

such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential.

14. The semiconductor device of Claim 6, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

15. The semiconductor device of Claim 7, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high

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P, 3734
figs. 15a, 15b

[illegible]

ductor device of claim 1, wherein said second terminal is supplied with a high potential, and said second threshold voltage is higher than said first threshold voltage, and wherein said first terminal is supplied with a high potential, and said first threshold voltage is higher than said second threshold voltage.

17. The semiconductor device of Claim 11, wherein:
said P-type semiconductor element is arranged in
such a manner that a threshold voltage becomes lower than
said low potential when said second input terminal is
supplied with said high potential, and lower than said
high potential and higher than said low potential when
said second input terminal is supplied with said low

Subt a^4

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

semiconductor device of Claim 1, wherein:
said semiconductor elements include an N-type semiconductor element and a P-type semiconductor element;
a first terminal of said N-type semiconductor element is supplied with a high potential;
said P-type semiconductor element is supplied with a low potential;
terminals of said P-type semiconductor element are connected to form a first input terminal;
terminals of said P-type semiconductor element are connected to form a second input terminal;
terminals of said P-type semiconductor element are connected to form a third input terminal;

fig. 16

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P-type semiconductor element
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substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

source terminals of said P-type semiconductor element and N-type semiconductor element are connected to

each other, thereby to form an output terminal.

19. The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a drain terminal of said N-type semiconductor element is supplied with a high potential and a drain terminal of said P-type semiconductor element is supplied with a low potential;

gate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a first input terminal;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

source terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

20. The semiconductor device of Claim 18, wherein

each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied

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figs. 17a, 17b

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Subtotal

$$\text{Subt } a^5$$

semiconductor device of Claim 1, wherein the
semiconductor elements
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terminal of said P-type
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fig. 18

a gate terminal of said N-type semiconductor element
and a substrate terminal of said P-type semiconductor

element are connected to each other, thereby to form a first input terminal;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

1/2 lot

^{source}
[drain] terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

23. The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is composed of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a drain terminal of said N-type semiconductor element and a low potential is supplied to a drain terminal of said P-type semiconductor element;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a

second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

24. The semiconductor device of Claim 22, wherein:

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P. 38, 79
figs. 19a, 19b

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

25. The semiconductor device of Claim 23, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal

is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

26. The semiconductor device of Claim 18, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

27. The semiconductor device of Claim 19, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that

a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

28. The semiconductor device of Claim 22, wherein:
said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low potential.

29. The semiconductor device of Claim 23, wherein:
said P-type semiconductor element is arranged in

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figs. 2, a, b
p. 42, 43

such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high potential and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low potential.

30. A semiconductor device comprising:

a semiconductor substrate;

a background insulating film formed over said semiconductor substrate;

figs. 4-6 a semiconductor layer of P- or N-type which is formed over said background insulating film and made into a first electrode, each element in said semiconductor layer being separated from an adjacent element by means of an insulating separation region which encircles each element;

a source region and a drain region which are formed

in said semiconductor layer and made into a second electrode and a third electrode, respectively, a conduction type of each being opposite to a conduction type of said semiconductor layer;

a channel region formed between said source region and drain region;

a gate insulating film formed over said channel region; and

a gate electrode formed as a fourth electrode on said gate insulating film,

said semiconductor device being characterized in that said semiconductor layer is separated by means of said separation region, and a contact hole is formed through said each semiconductor layer separated by means of said separation region, at a region other than said source region and drain region.

31. A semiconductor device comprising:

a semiconductor substrate;

a deep well region of P- or N-type formed in said semiconductor substrate;

figs. 7-9
a shallow well region which is formed over said deep well region and made into a first electrode, a conduction type of said shallow well region being opposite to a conduction type of said deep well region;

a source region and a drain region of P- or N-type which are formed in said shallow well region and made into a second electrode and a third electrode, respectively;

a channel region formed between said source region and drain region;

a gate insulating film formed over said channel region; and

a gate electrode formed as a fourth electrode on said gate insulating film,

said semiconductor device being characterized in that:

at least said shallow well region in each element is electrically separated from the shallow well region in an adjacent element by means of a separation region; and

a contact hole is provided to said shallow well region in each element separated from the shallow well region in the adjacent element by means of said separation region, at a region other than said source region and drain region.

32. The semiconductor device of Claim 30 or 31, wherein:

the elements having opposite conduction types are paired off;

a source of a P-type semiconductor element is fixed at a high potential and a source of an N-type semiconductor element is fixed at a low potential;

gates of both said P-type semiconductor element and N-type semiconductor element form a first input terminal;

said contact holes in both said P-type semiconductor element and N-type semiconductor element form a second input terminal; and

drains of both said P-type semiconductor element and N-type semiconductor element form an output terminal.

33. The semiconductor device of Claim 30 or 31, wherein:

the elements having opposite conduction types are paired off;

a source of a P-type semiconductor element is fixed at a high potential and a source of an N-type semiconductor element is fixed at a low potential;

a gate of said P-type semiconductor element and said contact hole in said N-type semiconductor element form a first input terminal;

both a gate of said N-type semiconductor element and said contact hole in said P-type semiconductor element form a second input terminal;

drains of both said P-type semiconductor element and

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N-type semiconductor element form an output terminal.

34. The semiconductor element of Claim 30 or 31, wherein:

the elements having opposite conduction types are paired off;

a drain of an N-type semiconductor element is fixed at a high potential and a drain of a P-type semiconductor element is fixed at a low potential;

gates of both said N-type semiconductor element and P-type semiconductor element form a first input terminal;

said contact holes in both said N-type semiconductor element and P-type semiconductor element form a second input terminal; and

sources of both said N-type semiconductor element and P-type semiconductor element form an output terminal.

35. The semiconductor element of Claim 30 or 31, wherein:

the elements having opposite conduction types are paired off;

a drain of an N-type semiconductor element is fixed at a high potential and a drain of a P-type semiconductor element is fixed at a low potential;

both a gate of said N-type semiconductor element

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